**Architecture of 80386**

•The Internal Architecture of 80386 is divided into 3 sections.

•Central processing unit

•Memory management unit

•Bus interface unit

•Central processing unit is further divided into Execution unit and Instruction unit

•Execution unit has 8 General purpose and 8 Special purpose registers which are either

used for handling data or calculating offset addresses.



•The **Instruction unit** decodes the opcode bytes received from the 16-byte instruction

code queue and arranges them in a 3- instruction decoded instruction queue.

•After decoding them pass it to the control section for deriving the necessary control

signals. The barrel shifter increases the speed of all shift and rotate operations.

• The multiply / divide logic implements the bit-shift-rotate algorithms to complete the

operations in minimum time.

•Even 32- bit multiplications can be executed within one microsecond by the multiply /

divide logic.

•The Memory management unit consists of a Segmentation unit and a Paging unit.

•Segmentation unit allows the use of two address components, viz. segment and offset for

relocability and sharing of code and data.

•Segmentation unit allows segments of size 4Gbytes at max.

•The Paging unit organizes the physical memory in terms of pages of 4kbytes size each.

•Paging unit works under the control of the segmentation unit, i.e. each segment is further

divided into pages. The virtual memory is also organizes in terms of segments and pages

by the memory management unit.

•The Segmentation unit provides a 4 level protection mechanism for protecting and

isolating the system code and data from those of the application program.

•Paging unit converts linear addresses into physical addresses.

•The control and attribute PLA checks the privileges at the page level. Each of the pages

maintains the paging information of the task. The limit and attribute PLA checks segment

limits and attributes at segment level to avoid invalid accesses to code and data in the

memory segments.

•The Bus control unit has a prioritizer to resolve the priority of the various bus requests.

This controls the access of the bus. The address driver drives the bus enable and address

signal A0 – A31. The pipeline and dynamic bus sizing unit handle the related control

signals.

•The data buffers interface the internal data bus with the system bus.